Confirmation no. 4587 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	SCHEUCHER, *et al.*	Examiner:	Quinto, K.
Serial No.:	10/584,504	Group Art Unit:	2826
Filed:	June 22, 2006	Docket No.:	AT030070US1
Title:	WAFER WITH OPTICAL CONTROL MODULES IN EXPOSURE FIELDS		

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No.
65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed September 4, 2008 and in response to the rejections of claims 1-7 as set forth in the Final Office Action dated June 13, 2008, and in further response to the Advisory Action dated August 5, 2008.

Please charge Deposit Account number 50-0996 (NXPS.440PA) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 018037/0384 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-7 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated June 13, 2008.

V. Summary of Claimed Subject Matter

Appellant's recited invention relates to segregation of semiconductor wafers by dicing, and to the positioning of alignment control modules to reduce the width of the dicing paths and thereby increase the usable wafer area.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a wafer (*see, e.g.*, wafer 1 shown in Fig. 1, along with page 4:31-34) that includes a number of exposure fields (*see, e.g.*, exposure fields 2 shown in Figs. 1 and 2, along with page 5:1-3) and a number of lattice fields (*see, e.g.*, lattice fields 3 shown in Fig. 2, along with page 5:5-7) in each exposure field, wherein each lattice field contains an IC (*see, e.g.*, integrated circuits 4 shown in Fig. 2, along with page 5:5-9), and where the wafer comprises a first group of dicing paths and a second group of second dicing paths (*see, e.g.*, dicing paths 6 shown in Fig. 1 and dicing path sections 6A, 6B, 6C, 8A, 8B, 8C, 8D shown in

Fig. 2, along with page 5:3-5), all of the first dicing paths of the first group run parallel to a first direction and have a first path width and all of the second dicing paths of the second group run parallel to a second direction intersecting the first direction and have a second path width (*see, e.g.*, directions X and Y shown in Fig. 1, along with page 5:10-15), the first dicing paths and the second dicing paths provided and designed for a subsequent segregation of the lattice fields and the ICs contained therein (*see, e.g.*, page 5:25-27), and wherein in each exposure field at least two control module fields are provided (*see, e.g.*, the four control module fields A1, A2, A3 and A4 shown in a single exposure field 2 in Fig. 2, along with page 6:31-33) such that the control module fields do not reside in any of the dicing paths (*see, e.g.*, Fig. 2 generally, along with page 3:18-22), each of the control module fields containing at least one optical control module (*see, e.g.*, optical control modules OCM-A1, OCM-A2, and so forth as shown in Fig. 2, along with page 6:22-30), and each control module field provided in an exposure field in place of a preset number of lattice fields (*see, e.g.*, Fig. 2 generally, along with page 7:32 through page 8:7), and wherein the at least two control module fields of each exposure field are arranged at an average distance from one another extending in the second direction equal to at least a quarter of the side length of a side of the exposure field which extends in the second direction (*see, e.g.*, Fig. 2 generally, along with page 7:1-10).

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1-6 stand rejected under 35 U.S.C. § 102(b) over Watanabe *et al.* (US Patent No. 5,721,091.

B. Claim 7 stands rejected under 35 U.S.C. § 103(a) over Watanabe.

VII. Argument

Appellant submits that the rejections of claims 1-7 over the Watanabe reference cannot be allowed to stand because Watanabe fails to teach or suggest numerous features recited in Appellant's claims. In particular, Appellant submits that Watanabe appears to disclose none of the claimed features relevant to wafer dicing, including structural features relating to dicing paths and exposure fields (exposure fields including the IC components, and dicing paths being the unused area located between exposure fields for wafer dicing and chip segregation), control fields that do not reside in any dicing paths (control fields including the control modules for alignment), and control modules that displace a preset number of lattice fields (lattice fields containing the IC components). Appellant submits that Watanabe fails to discuss these features because the Watanabe reference appears to be wholly unrelated to wafer dicing, instead being directed to a resist composition that prevents charging during ion implantation processes.

As set forth in the discussions that follow, Appellant submits that the Examiner has misinterpreted and misapplied the Watanabe reference to wafer dicing, including the structural features described and claimed by Appellant. Instead, the cited portions of Watanabe relate to an arrangement for testing whether a coating of a photoresist composition on a wafer is sufficiently resistant to electrical charging, and which fails to teach many of Appellant's claimed features. It appears to Appellant that the Examiner's misinterpretation of Watanabe is predicated on affording improper weight to several features of Appellant's claims as relating to the "operation of the claimed structures" (*see* Advisory Action), thus improperly disregarding the recited subject matter. *See*, M.P.E.P. 2173.05(g). For example, the Examiner fails to

address the deficiency that dicing paths are in no manner shown or discussed in Watanabe. Furthermore, the Examiner fails to address the deficiency that optical control modules are in no manner shown or discussed in Watanabe. Without support for these structural elements, the rejections are left without foundation.

In semiconductor wafer manufacturing, multiple integrated circuits are patterned onto a wafer and divided into chips along a number of scribe lines, or dicing paths. Alignment marks are used to ensure that patterning of the integrated circuits occurs in the correct areas, called exposure fields. In known systems, the widths of the dicing paths (which include the unused area in between the exposure fields), depend on the placement of the alignment marks. Appellant's invention recognizes that the wasted wafer area from the dicing paths and alignment mark placement can be reduced by removing the dependence of dicing path width on the alignment marks. In particular, Appellant's invention involves placing optical control modules used for alignment within the exposure fields of the wafer, and displacing a portion of the IC area with the alignment control modules. Appellant appreciated that the wafer area "cost" of displacing ICs with alignment control modules can be substantially outweighed by gains in usable area realized by the resulting narrower dicing paths (*see, e.g.*, page 2:30 through page 3:22 of Appellant's Specification). The Examiner has presented no evidence, including in the Watanabe reference or other art of record, that such features as taught and claimed by Appellant were known prior to Appellant's invention. Moreover, the Examiner has not articulated any reason why one of skill in the art would seek to implement these features.

Therefore, and for the reasons detailed in the following discussions, Appellant requests that the Board reverse the rejections as improper and unsupported by the art.

A. The § 102(b) rejection of claims 1-6 is improper because Watanabe does not disclose numerous features recited in Appellant's claims.

In order to sustain a rejection under § 102, the applied reference must disclose each and every element recited in the rejected claims. *See,* M.P.E.P. § 2131. The Examiner has failed to meet this burden, and in fact has failed to demonstrate correspondence in the Watanabe reference for any of the claim features identified by the Examiner. For example, Appellant finds nothing in the Watanabe reference to teach the features of: dicing paths; control module fields

including optical control modules for alignment of the dicing paths and exposure fields; control module fields residing in the exposure fields and not residing in any of the dicing paths; or control module fields provided in place of a preset number of IC-containing lattice fields. The failure to disclose any of these features is fatal to the § 102 rejection, and Watanabe discloses none of them.

As understood by Appellant, the Watanabe reference is unrelated to the wafer dicing subject matter recited in Appellant's claims. Instead, Watanabe teaches a resist composition that prevents charging during certain processing steps such as ion implantation. As explained by Watanabe, misalignment can occur during resist-based patterning processes when the resist material takes on an electrical charge (*see, e.g.*, Watanabe Col. 2:58-66). The portions of Watanabe cited by the Examiner, and in particular Figs. 7A-7E, describe how Watanabe evaluated the disclosed methods for preventing charge-up of the photoresist material, including the use of electron-beam detectable alignment marks to check for mis-registration or other dimensional errors after exposing the photoresist layer to an electron beam (*see, e.g.*, Watanabe Col. 11:65 through Col. 12:18). As the following discussion details, not only does Watanabe fail to show dicing paths and optical control modules as claimed, but one of skill in the art would recognize that, were the "chips" indicated in Fig. 7E to be segregated, it would be along the chips' edges, thus overlapping Watanabe's alignment marks, in clear distinction to Appellant's claims.

1. Watanabe fails to disclose dicing paths for wafer segregation, as claimed.

As discussed, the Watanabe reference does not discuss dicing operations, and therefore does not disclose or in any way indicate dicing paths as claimed by Appellant. As explained by Appellant, dicing paths are defined by the width of the unused area between adjacent exposure fields, for example widths W1 and W2 shown in Fig. 2 (*see, also*, page 5:10-27). While the Examiner cites to Figs. 7A-7E of Watanabe as generally showing "a structure which meets the claims" (*see*, page 2 of Final Office Action), Appellant notes that no specific correspondence is found for the claimed dicing paths. Moreover, Appellant observes that Figs. 7A-7E are described as showing a test arrangement, which includes many chips on an Al-Si wafer, to

evaluate whether certain photoresist materials are susceptible to charging effects. The degree of charging was determined by comparing detected alignment mark positions before and after exposure of the photoresist to an electron beam (*see, e.g.*, Watanabe Col. 11:65 through Col. 12:18). As such, not only does Watanabe fail to indicate any dicing paths on the wafer, the arrangement of chips and alignment marks shown in Figs. 7A-7E are specifically provided for the purpose of testing photoresist charging, and not for wafer manufacture and segregation operations.

Appellant therefore requests that the § 102 rejection be reversed as improper because Watanabe fails to disclose dicing paths, as claimed.

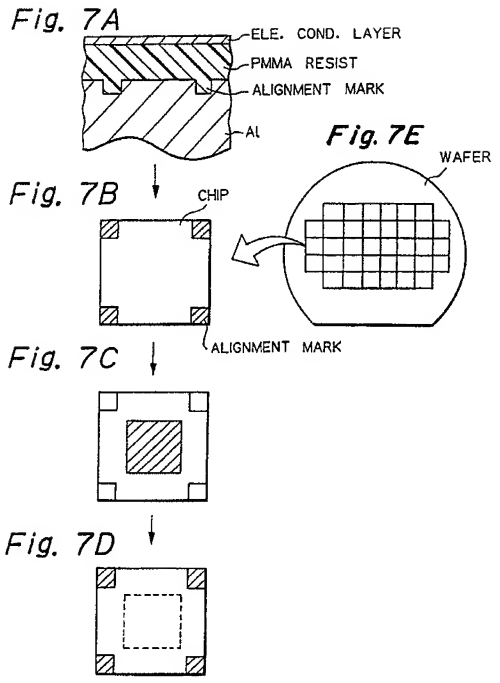
2. Watanabe fails to disclose control module fields including optical control modules for dicing and exposure field alignment, as claimed.

Appellant further submits that Watanabe fails to disclose the use of optical control modules as described and claimed. As Appellant explains, optical control modules are used in wafer dicing operations for mask adjustment and layer thickness testing, and contain square or rectangular interference fields that are optically detectable by the naked eye or by computer-aided detection devices (*see, e.g.*, page 6:3-9 of Appellant's Specification). As discussed, the alignment marks disclosed by Watanabe are not used for wafer dicing, but rather are disclosed for the purpose of detecting photoresist charging, which Watanabe discloses exhibit misalignment effects. Moreover, Watanabe clearly discloses that the alignment marks are detected using an electron beam (*see, e.g.*, Col. 12:7-10), and therefore cannot be correlated to the optically-detectable optical control modules described and claimed by Appellant.

Appellant therefore requests that the § 102 rejection be reversed as improper because Watanabe fails to disclose optical control modules, as claimed.

3. Watanabe fails to disclose control module fields residing in the exposure fields and not residing in any of the dicing paths, as claimed.

Appellant further submits that Watanabe fails to disclose a wafer in which the control module fields for dicing alignment reside in the exposure fields and not in any of the dicing paths, as claimed. As discussed, Watanabe does not teach dicing operations, dicing paths, or optical control modules for alignment during dicing. Thus, it is difficult for Appellant to understand what the Examiner considers to correspond to the claimed exposure fields and dicing paths. Clearly, the Examiner's rejection is based on the (erroneous) interpretation that Watanabe's alignment marks correspond to the claimed control module fields. The Examiner has nonetheless failed to demonstrate that Watanabe's alignment marks reside within exposure fields (not identified), or that Watanabe's alignment marks do not reside in any dicing paths (not identified). It appears to Appellant that the Examiner is saying it is inherent or implicit that Watanabe's alignment marks would reside outside of the dicing paths. This is demonstrably untrue. Appellant submits that the electron beam exposure performed by Watanabe for evaluating the extent of photoresist charging is confined to a central region of the chip, shown shaded in Fig. 7C (reproduced below), which does not include the alignment marks. Moreover, the alignment marks appear to be coincident with the edges of the chip where dicing paths would be found (although none are shown by Watanabe).



Figs. 7A-7E of Watanabe

Appellant therefore submits that the Watanabe reference provides no teaching or disclosure to lead one of skill in the art to conclude that the disclosed alignment marks could be interpreted as control module fields residing in exposure fields and not residing in any dicing paths, as claimed. Thus, Appellant requests that the § 102 rejection be reversed as improper.

4. Watanabe fails to disclose control module fields provided in place of a preset number of IC-containing lattice fields, as claimed.

Appellant further submits that Watanabe fails to disclose control module fields positioned to displace a preset number of lattice fields, as claimed. As discussed, there is no teaching in the Watanabe reference that mentions any application to dicing operations, much less that teaches or suggests that the disclosed alignment marks could somehow be construed as optical control modules that replace a present number of IC-containing lattice fields, as claimed. Moreover, the Examiner has failed to identify any disclosure in Watanabe of alignment control modules displacing lattice fields or ICs contained therein. While the Final

Office Action includes a reference to "lattice fields (3b)," Appellant is unable to find any item labeled or identified as "3b" within the Watanabe reference. It appears that "lattice fields (3b)" is a left-over reference to the Tsuji document (U.S. Pat. No. 6,005,294) applied by the Office Action of December 17, 2007, and apparently overcome by Appellant's Response of March 12, 2008. Appellant therefore submits that the Examiner has provided no basis for the Watanabe reference teaching control module fields displacing lattice fields, as claimed. Thus, Appellant requests that the § 102 rejection be reversed as improper.

B. The § 103(a) rejection of claim 7 is improper because Watanabe does not disclose numerous features recited in Appellant's claims, and because Watanabe is unrelated to wafer dicing.

The Examiner admits that Watanabe does not disclose three different groups of dicing paths running in different directions on a wafer as claimed in claim 7, but nonetheless considers the inclusion of a third dicing path to be an obvious variation. Appellant submits, however, that the § 103(a) rejection is improper for failure to address the severe and numerous deficiencies of the Watanabe reference as applied to claim 1 and as discussed above. Moreover, because Watanabe clearly has no application to the claimed wafer dicing operations, Appellant submits that the Examiner's conclusion of obviousness is mere conjecture, unsupported by any evidence on the record. For at least these reasons, Appellant requests that the § 103 rejection be reversed as improper.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-7 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: _____

Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.440PA)

APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/584,504)

1. A wafer, which wafer comprises a number of exposure fields and which wafer comprises a number of lattice fields in each exposure field, wherein each lattice field contains an IC, and which wafer comprises a first group of dicing paths and a second group of second dicing paths, wherein all of the first dicing paths of the first group run parallel to a first direction and have a first path width and wherein all of the second dicing paths of the second group run parallel to a second direction intersecting the first direction and have a second path width and wherein the first dicing paths and the second dicing paths are provided and designed for a subsequent segregation of the lattice fields and the ICs contained therein, and wherein in each exposure field at least two control module fields are provided such that the control module fields do not reside in any of the dicing paths, each of which control module fields contains at least one optical control module, and wherein each control module field provided in an exposure field is provided in place of a preset number of lattice fields and wherein the at least two control module fields of each exposure field are arranged at an average distance from one another extending in the second direction which average distance is equal to at least a quarter of the side length of a side of the exposure field which extends in the second direction.

2. A wafer as claimed in claim 1, wherein the average distance is equal to the whole side length of a side of the exposure field which extends in the second direction minus the side length of a side of a lattice field which extends in the second direction.

3. A wafer as claimed in claim 1, wherein each exposure field is designed rectangular, and wherein four control module fields are provided in each exposure field, and wherein each control module field is located in a corner region of the exposure field in question.

4. A wafer as claimed in claim 1, wherein each control module field, provided in an exposure field is provided in place of one lattice field only.

5. A wafer as claimed in claim 1, wherein the dicing paths are free of any control module fields.

6. A wafer as claimed in claim 1, wherein the dicing path widths are determined solely by equipment used to segregate the wafer.

7. A wafer as claimed in claim 1, further comprising a third group of dicing paths that run parallel to a third direction intersecting both the first direction and the second direction.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.